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10/038,998	01/05/2002	Randy J. King	C17767/127288	7470

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EXAMINER	
JONES III, CLYDE H	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,998	KING ET AL.	
	Examiner	Art Unit	
	Clyde H. Jones III	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 March 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/11/02; 9/06/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 3, 6, 7 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (US 5,978,389).

In regards to claim 1, Chen teaches –

A video switch (30 - Fig. 3 or 40 – Fig. 4A-4C) for switching a video output (R, G, B outputs) of one of a plurality of computers (computers a-d) to a target video destination (monitor 36 – Fig. 3 or 46 – Fig. 4), the video switch comprising:

a voltage converter having an input and an output (voltage amplifying circuit 3411 – Fig. 3 or 4411 – Fig. 4A), wherein a video select signal (S31, S32 – Fig. 3 or S41, S42 – Fig. 4) is operably connected (i.e., connected so the circuit is operable) to the input of the voltage converter; and

a discrete radio frequency switch (31, 32, 33 – Fig. 3 or 41, 42, 43 & D1-D12 – Fig. 4A-4C; col. 6, lines 17-18) having a control (37- Fig. 3 or 47 - Fig. 4), a video input (Ra-Rd, Ga-Gd, Ba-Bd) and a video output (monitor 36 - Fig. 3 or 46 - Fig. 4), wherein the video output of one of the plurality of computers is operably connected to the video input of the discrete radio frequency switch (col. 3, lines 31-40; col. 4, lines 35-47),

wherein the output of the voltage converter is operably connected (i.e., connected so the circuit is operable) to the control of the discrete radio frequency switch (col. 3, lines 12-59).

Regarding claims 2 and 3, Chen teaches the voltage converter comprises a resistor divider operably connected to a logic device (col. 4, lines 36-58 & Fig. 4A; in which the voltage amplifying circuit comprises a voltage divider RH and RL, or R9 and R10, to provide a voltage bias for which the diode switches (diodes D1–D4) can compare to control signals Ca-Cd to determine which video signal should be selected to be input to the next section, e.g., the anodes of diodes D1-D4 are biased around 1.8 V and Cb is at 0 volts while the other control signals are +5 volts, therefore the diode D2 detects a forward bias on the Rb line and allows signal Rb to conduct to the next section; as to the further limitation "comparator" or "logic device", it reads on Chen's diode switch which compares two voltages and switches its output to indicate which is larger).

In regards to claim 6, Chen teaches the video output is operably connected to a peaking video amplifier circuit (3411- Fig. 3 or 4411 – Fig. 4; col. 5, lines 18-45; col. 6, lines 7-16; which reads on "peaking amplifier", in which circuit 3411 or 4411 amplifies the video signals in order to compensate for high frequency transmission attenuation or distortion).

In regards to claim 7, Chen teaches –

a video switch (30 - Fig. 3 or 40 – Fig. 4A-4C) comprising:

a plurality of switch circuits configured into a multiplexed circuit (31, 32, 33 – Fig. 3 or 41 - Fig. 4A, 42 – Fig. 4B, and 43 – Fig. 4C), wherein at least one switch circuit of said plurality of switch circuits comprises a discrete radio frequency switch (diode switches D1-D12 – Fig. 4A-4C; col. 6, lines 7-18) having a control input (Ca-Cd) and voltage converter (3411, Fig. 3 or 4411– Fig. 4A) operably connected to the control input of the discrete radio frequency switch (col. 3, lines 12-59).

In regards to claim 9, Chen teaches-

A video switch (30 - Fig. 3 or 40 – Fig. 4A-4C) for connecting the video signals of one of a plurality of computers (R, G, B outputs) to a target monitor (monitor 36 – Fig. 3 or 46 – Fig. 4), said video switch comprising:

three sets of switch circuits for receiving red, green, blue video signals of said plurality of computers respectively (31, 32, 33 – Fig. 3; 41, 42, 43 – Fig. 4A-4C), each set of switch circuits comprising a plurality of discrete radio frequency switches (diode switches D1-D12 – Fig. 4A-4C; col. 6, lines 7-16) , the number of said plurality of discrete radio frequency switches being no less than the number of said plurality of target monitors (Chen shows twelve diode switches for one target monitor 46 – Fig. 4); and

a control signal generating circuit (37 – Fig. 3 or 47 – Fig. 4) having a video selecting signal as an input (S31 and S32 – Fig. 3 or S41 and S42 – Fig. 40), and

generating a plurality of control signals (Ca, Cb, Cc, Cd), the number of said plurality of control signals being no less than the number of said plurality of computers (Chen shows four control signals generated for four computer a, b, c, and d – Fig. 3 or 4), each of said plurality of control signals coupled to a voltage-level shifting circuit (inherently disclosed inside 37 - Fig. 3 or 47 – Fig. 4; col. 4, lines 35-47; in which the control signal generating circuit inherently has a voltage-level shifting circuit to provide the 0 volt or +5 volt levels for the control signals Ca-Cd as disclosed), the output of the voltage-level shifting circuit being used for controlling each corresponding discrete radio frequency switch (D1-D12 – Fig. 4A-4C) in said three sets of switch circuits (31, 32, 33 – Fig. 3 or 41, 42, 43 – Fig. 4A-4C) (col. 6, lines 17-18; col. 4, lines 48-58; in which voltage-level shifted outputs Ca-Cd (at 0 volt or +5 volts) controls each discrete radio frequency switch).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,978,389) in view of McWhorter et al. (Basic Electronics).

Regarding claims 4 and 8, Chen discloses using a set of diode switch circuits (31, 32, 33 – Fig. 3), which when the control signals (Ca–Cd) is positive +5 volts the corresponding video signal (Ra – Rd) does not conduct and when one of the control signal is 0 volts the corresponding video signal conducts, i.e., the signal the user selects for monitoring will have a corresponding control voltage of 0 volts (col. 4, lines 36-59). Chen further discloses "suitable transistors" can be used because they are not complicated and will not generate too much noise (col. 3, line 60 – col. 4, line 5).

Chen fails to disclose the limitation "the discrete radio frequency switch is a depletion mode MOSFET device".

However in an analogous art McWhorter teaches a P-channel MOSFET that only conducts the source/input signal when the gate/control voltage is low, i.e., not "increasingly high", e.g., 0 volts is applied to the gate of the depletion mode P-channel MOSFET and it conducts from source to drain, and in an alternative example, when +5 volts is applied to the gate it does not conduct from the source to the drain (page 82, lines 30-35; Fig. 4-18, page 83).

It would be obvious to one skilled in the art at the time the invention was made to modify the system of Chen to include the limitation "the discrete radio frequency switch is a depletion mode MOSFET device" as disclosed by McWhorter to implement an input selection switch which is not complicated and will not generate a lot of noise (Chen – col. 4, lines col. 3, line 67- col. 4, line 5), furthermore it is well known in the art that

depletion mode P-channel MOSFETs can be used for switching and they are readily available commercially.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,978,389) in view of Matsubara et al. (US 2003/0001966 A1).

In regards to claim 5, Chen teaches-

A video switch (30 - Fig. 3 or 40 – Fig. 4A-4C) for switching a video output (R, G, B outputs) of one of a plurality of computers (computer a-d) to a target video destination (monitor 36 – Fig. 3 or 46 – Fig. 4), the video switch comprising:

a first logic gate (inherently inside 37 – Fig. 3 or 47 – Fig. 4A-4C) having a video control input (S31, S32 – Fig. 3 or S41, S42 – Fig. 4), and a control output (Ca, Cb, Cc or Cd), the control output of the first logic gate having a first voltage level (0 or +5 volts) (col. 4, lines 36-47; col. 3, lines 33-35; in which Chen discloses a decoder control signal generating circuit, i.e., a n-to-2n decoder which inherently uses combinational logic, e.g., a plurality of AND, OR, NOR, NAND, or NOT gates, etc., to convert the coded inputs, i.e., S31, S32 or S41, S42, into the decoded outputs, i.e., Ca, Cb, Cc or Cd, as disclosed);

a resistor divider network operably coupled to the control output of the first logic gate (col. 4, lines 36-58 & Fig. 4A; in which voltage divider RH and RL, and R9 and R10, provide a voltage bias for which the diode switches (diodes D1–D4) can compare to the control output signals Ca-Cd to determine which video signal should be selected to be conducted to the next section, e.g., the anodes of diodes D1-D4 are biased

around 1.8 V and first output Cb is at 0 volts (when it is selected by S41 & S42 or S31 & S32) while the other control signals are +5 volts, therefore the diode D2 detects a forward bias and allows only the Rb line to conduct to the next section);

a second logic gate (inherently inside 37 – Fig. 3 or 47 – Fig. 4A-4C) operably coupled to the resistor divider network, the second logic gate having a control output, the control output of the second logic gate having a second voltage level (reads on a second output voltage (0 or +5 volts) of the plurality of outputs being generated from a second logic gate (of the plurality of logic gates inherently disclosed inside 37 or 47 as described above) being compared to the bias voltage provided by the resistor divider, e.g., the video select signals make 37 or 47 output 0 volts for a first output Cb and +5 volts for a second output Ca, thereby causing video signal b to conduct while video signal a doesn't conduct);

a discrete radio frequency switch (31, 32, 33 – Fig. 3 or 41, 42, 43 & D1-D12 – Fig. 4A-4C; col. 6, lines 17-18) having a control (37- Fig.3 or 47-Fig. 4), a video input (Ra-Rd, Ga-Gd, Ba-Bd) and a video output (monitor 36 - Fig. 3 or 46 - Fig. 4), wherein the video output of one of the plurality of computers is operably connected to the video input of the discrete radio frequency switch (col. 3, lines 31-40), wherein the control output of the second logic gate (Ca continuing from the previous example) is operably connected to the control of the discrete radio frequency switch (e.g. control output Ca of the inherently disclosed second logic gate, is operably connected to control the conduction of video signal a through select diodes in the diode switch).

Chen fails to disclose the further limitation "OSD control input".

In an analogous art Matsubara discloses an "OSD control input" ("command") (Fig. 4; Fig. 5; pg. 6, par. 90, line 7 – par. 92, line 7; in which Matsubara discloses the OSD control input/command is used to generate an OSD screen corresponding to the selected computer upon activation of selection/operation switch 8 – Fig. 4, e.g. a user activates switch 8 to switch from computer 2A to computer 2B and an OSD screen is switched to, i.e., displayed, corresponding to the user's selection).

It would have been obvious to one skilled in the art at the time the invention was made to modify the system of Chen to include the limitation "OSD control input" as taught by Matsubara to provide information to the user regarding what video signal of the plurality of computers is active, i.e., currently displayed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clyde H. Jones III whose telephone number is 571-272-5946. The examiner can normally be reached on 9-5:30 p.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Grant can be reached on 571-272-7294. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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